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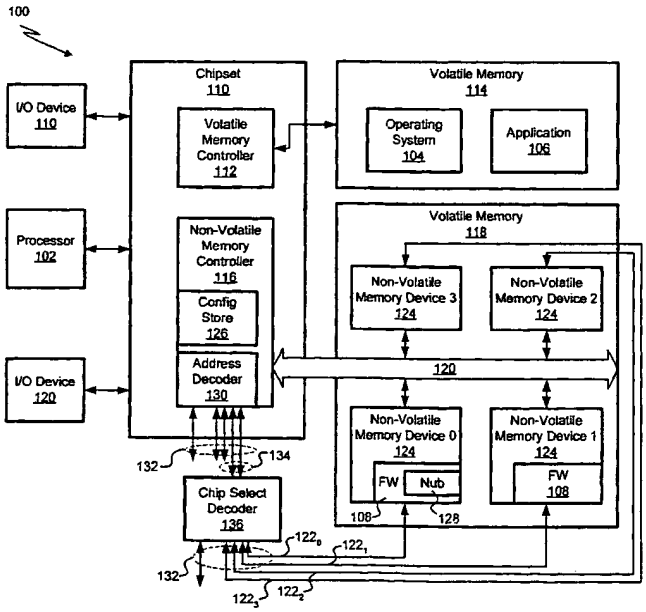
[Continued on next page]

(54) Title: PROGRAMMABLE CHIP SELECT



(57) Abstract: Machine-readable media, methods, and apparatus that generate chip selects words (132) are disclosed. In one embodiment, an address decoder (130) may generate an encoded chip select word to select a memory device (124) when in an encoded chip select mode. The address decoder may also generate an unencoded chip select word to select a memory device when in an unencoded chip select mode. In one embodiment, the address decoder, in response to an address for a boot code nub (128), may generate a chip select word that selects the same memory device regardless of whether the address decoder is operating in an encoded or unencoded chip select mode.

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PROGRAMMABLE CHIP SELECT

BACKGROUND

[0001] A computing device may comprise firmware routines to initialize components of the computing device. Upon system startup, the computing device may activate a chip select of a non-volatile memory device having the firmware routines. The computing device may then retrieve and execute the firmware routines from the non-volatile memory device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The invention described herein is illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, elements illustrated in the figures are not necessarily drawn to scale. For example, the dimensions of some elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

[0003] FIG. 1 illustrates an embodiment of a computing device without a chip select decoder.

[0004] FIG. 2 illustrates an embodiment of a computing device with a chip select decoder.

[0005] FIG. 3 illustrates a startup method that the computing devices of FIG. 1 and FIG. 2 may execute.

which may be read and executed by one or more processors. A machine-readable medium may include any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computing device). For example, a machine-readable medium may include read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other forms of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); and others. Further, firmware, software, routines, instructions may be described herein as performing certain actions. However, it should be appreciated that such descriptions are merely for convenience and that such actions in fact result from computing devices, processors, controllers, or other devices executing the firmware, software, routines, instructions, etc.

[0009] Example embodiments of a computing device 100 are shown in FIG. 1 and FIG. 2. As illustrated, the computing device 100 may comprise one or more processors 102. The processors 102 may perform actions in response to executing instructions of an operating system 104, application 106, basic input/output system (BIOS) firmware 108, and/or some other software or firmware module.

[0010] The computing device 100 may further comprise a chipset 110 that is coupled to the processors 102 via a processor bus. The chipset 110 may comprise one or more integrated circuit packages or chips that couple the processors 102 to other components of the computing device 100. In particular, the chipset 110 may comprise a volatile memory controller 112 that is coupled to volatile memory 114 via a memory bus. The chipset 110 may further comprise a non-volatile memory controller 116 that is coupled to a non-volatile memory 118

controller 116. In one embodiment, the configuration store 126 may configure the non-volatile memory controller 116 for an encoded chip select mode or an unencoded chip select mode. Moreover, the configuration store 126 may configure the non-volatile memory controller 116 for various non-volatile memory configurations. For example, the non-volatile memory controller 116 via the configuration store 126 may support multiple memory types, memory capacities, memory timings, etc.

[0014] In one embodiment, the configuration store 126 may default the non-volatile memory controller 116 to an encoded chip select mode. The configuration store 126 may further default the non-volatile memory controller to a memory configuration that assumes a non-volatile memory device 118 coupled to a predetermined chip select line 122 (e.g. chip select line 122_0), that the non-volatile memory device 118 consists of a minimum storage capacity (e.g. 1 megabyte) supported by the non-volatile memory device 124, that maps a boot code nub address to a boot code nub 128 stored in a predetermined non-volatile memory device 118, and that rolls over addresses to the predetermined non-volatile memory device 124 to ensure all addresses target the predetermined non-volatile memory device 124 until configured otherwise.

[0015] The non-volatile memory controller 116 may comprise an address decoder 130 to decode an address into a chip select word that selects a non-volatile memory device 124 to service a transaction, into a row address that selects the appropriate row of the selected non-volatile memory device 124, and a column address that selects the appropriate column of the selected row. In response to the unencoded chip select mode, the non-volatile memory controller 116 may generate an unencoded chip select word 132 (FIG. 1). The address

to the chip select line 122_X. Moreover, a binary 0 in TABLE 1 indicates an inactive bit of the chip select word and a binary 1 indicates an active bit of the chip select word. An active bit may correspond to a high signal and an inactive bit may correspond to a low signal. However, other signal encodings may be used such as, for example, representing an active bit with a low signal and an inactive bit with a high bit.

[0018]

	Encoded Chip Selects CS[2:0]	**Unencoded Chip Selects CS[7:0]**
CS_Word_0	001b	0000_0001b
CS_Word_2	010b	0000_0010b
CS_Word_2	011b	0000_0100b
CS_Word_3	100b	0000_1000b
CS_Word_4	101b	0001_0000b
CS_Word_5	110b	0010_0000b
CS_Word_6	111b	0100_0000b
CS_Word_7	000b	1000_0000b

TABLE 1

[0019] As illustrated in TABLE 1, the three lowest order bits [2:0] of the encoded chip select word CS_Word_0 and the three lowest order bits [2:0] of the unencoded chip select word CS_Word_0 are the same and include a single active bit. Assuming a valid platform, the address decoder 130 may select the non-volatile memory device 124 coupled to chip select line 122_0 by generating the unencoded chip select word CS_Word_0 or the encoded chip select word CS_Word_0. For example, if the computing device 100 does not include a chip

[0021] As depicted in FIG. 1, the boot code nub 128 may reside in a non-volatile memory device 124 associated with a predetermined chip select line (e.g. chip select line 122_0). Moreover, the computing device 100 of FIG. 1 depicts that the BIOS firmware 108 may span more than one non-volatile memory device 124. In one such embodiment, the computing device 100 may executed the boot code nub 128 in order to configure the non-volatile memory controller 118 and enable access to the other non-volatile memory devices 124 and startup routines of the BIOS firmware 108 that reside in the other non-volatile memory devices 124. However, in other embodiments, the BIOS firmware 108 may reside in a single non-volatile memory device 124.

[0022] The chipset 110 may further comprise input/output (I/O) controllers (not shown) coupled to I/O devices 138 (e.g. a mouse, keyboard, video controller, network interface controller, hard disk, floppy disk, wireless receivers, wireless transmitters, etc.) via buses. For example, the chipset 110 may comprise peripheral component interconnect (PCI) controllers, accelerated graphics port (AGP) controllers, universal serial bus (USB) controllers, low pin count (LPC) bus controllers, and/or other input and/or output (I/O) controllers to control and transfer data via the respective buses.

[0023] Referring now to FIG.3, there is shown a startup method that the computing device 100 of FIG. 1 or FIG. 2 may perform in response to a system power-up, a system reset, or some other event. The processor 102 in block 200 may jump to a boot code nub address (e.g. FFFF_FFFFh). The address decoder 130 may decode the boot code nub address and generate a chip select word 132, 134 (e.g. unencoded or encoded chip select word CS_Word_0) having a single active bit to select the predetermined non-volatile memory device 124 that

unencoded chip select mode if the processor 102 determines that the computing device 100 does not include a chip select decoder.

[0026] Moreover, processor 102 may update the configuration store 126 to configure the non-volatile memory controller 116 for the types and capacities of the non-volatile memory devices 124 detected by the processor 102 in response to executing the boot code nub 128. The processor 102 may further update the configuration store 126 to disable rolling addresses over to the predetermined non-volatile memory device 124 that comprises the boot code nub 128. After configuring the non-volatile memory controller 116, the processor 102 in response to executing the boot code nub 128 or the BIOS firmware 108 may reassign unused chip select pins for other purposes, such as, a General Purpose Event (GPE).

[0027] While certain features of the invention have been described with reference to example embodiments, the description is not intended to be construed in a limiting sense. Various modifications of the example embodiments, as well as other embodiments of the invention, which are apparent to persons skilled in the art to which the invention pertains are deemed to lie within the spirit and scope of the invention.

5. The apparatus of claim 1 wherein the address decoder, in response to an address for a boot code nub,

generates the encoded chip select word for the address such that the encoded chip select word comprises exactly one active chip select bit, and

generates the unencoded chip select word for the address such that the unencoded chip select word comprises exactly one active chip select bit.

6. The apparatus of claim 1 wherein the address decoder, in response to an address for a boot code nub,

generates the encoded chip select word for the address such that the encoded chip select word comprises exactly one active chip select bit that corresponds to a predetermined chip select line used to select a memory device comprising the boot code nub, and

generates the unencoded chip select word for the address such that the unencoded chip select word comprises exactly one active chip select bit that corresponds to the predetermined chip select line.

7. The apparatus of claim 1 wherein the address decoder, in response to an address for a boot code nub,

generates the encoded chip select word such that a lowest order bit of the encoded chip select word is the only active bit of the encoded chip select word, and

generates the unencoded chip select word such that a lowest order bit of the unencoded chip select word is the only active bit of the unencoded chip select word.

8. A system comprising

12. The system of claim 8 further comprising a chip select decoder coupled to the apparatus and coupled to each of the memory devices of the plurality of memory devices via a separate chip select line, wherein

the chip select decoder activates the chip select line of the memory device with the boot code nub in response to receiving the encoded chip select word for the address of the boot code nub from the unencoded chip select word generated by the apparatus for the address of the boot code nub.

13. A method comprising

generating, in response to an address of a boot code nub and an encoded chip select mode, an encoded chip select word that selects a memory device with the boot code nub, and

generating, in response to the address of the boot code nub and an unencoded chip select mode, an unencoded chip select word that comprises the encoded chip select word of the boot code nub.

14. The method of claim 13 further comprising

updating an operation mode to one of the encoded chip select mode and the unencoded chip select mode.

15. The method of claim 13 further comprising

executing the boot code nub, and

updating an operation mode to one of the encoded chip select mode and the unencoded chip select mode in response to executing the boot code nub.

16. The method of claim 13 further comprising

executing the boot code nub,

updating an operation mode to the encoded chip select mode in response to executing the bood code nub, and

20. A machine readable medium comprising a plurality of instructions that, in response to being executed result, in an apparatus

generating, in response to an address of a boot code nub and an encoded chip select mode, an encoded chip select word that selects a memory device with the boot code nub, and

generating, in response to the address of the boot code nub and an unencoded chip select mode, an unencoded chip select word that comprises the encoded chip select word of the boot code nub.

21. The machine readable medium of claim 20 wherein the plurality of instructions further result in the apparatus

generating the encoded chip select word such that the encoded chip select word comprises exactly one active chip select bit, and

generating the unencoded chip select word such that the unencoded chip select word comprises exactly one active chip select bit.

22. The machine readable medium of claim 20 wherein the plurality of instructions further result in the apparatus

generating the encoded chip select word such that the encoded chip select word comprises exactly one active chip select bit that corresponds to a predetermined chip select line used to select the memory device with the boot code nub, and

generating the unencoded chip select word such that the unencoded chip select word comprises exactly one active chip select bit that corresponds to the predetermined chip select line.

23. The machine readable medium of claim 20 wherein the plurality of instructions further result in the apparatus

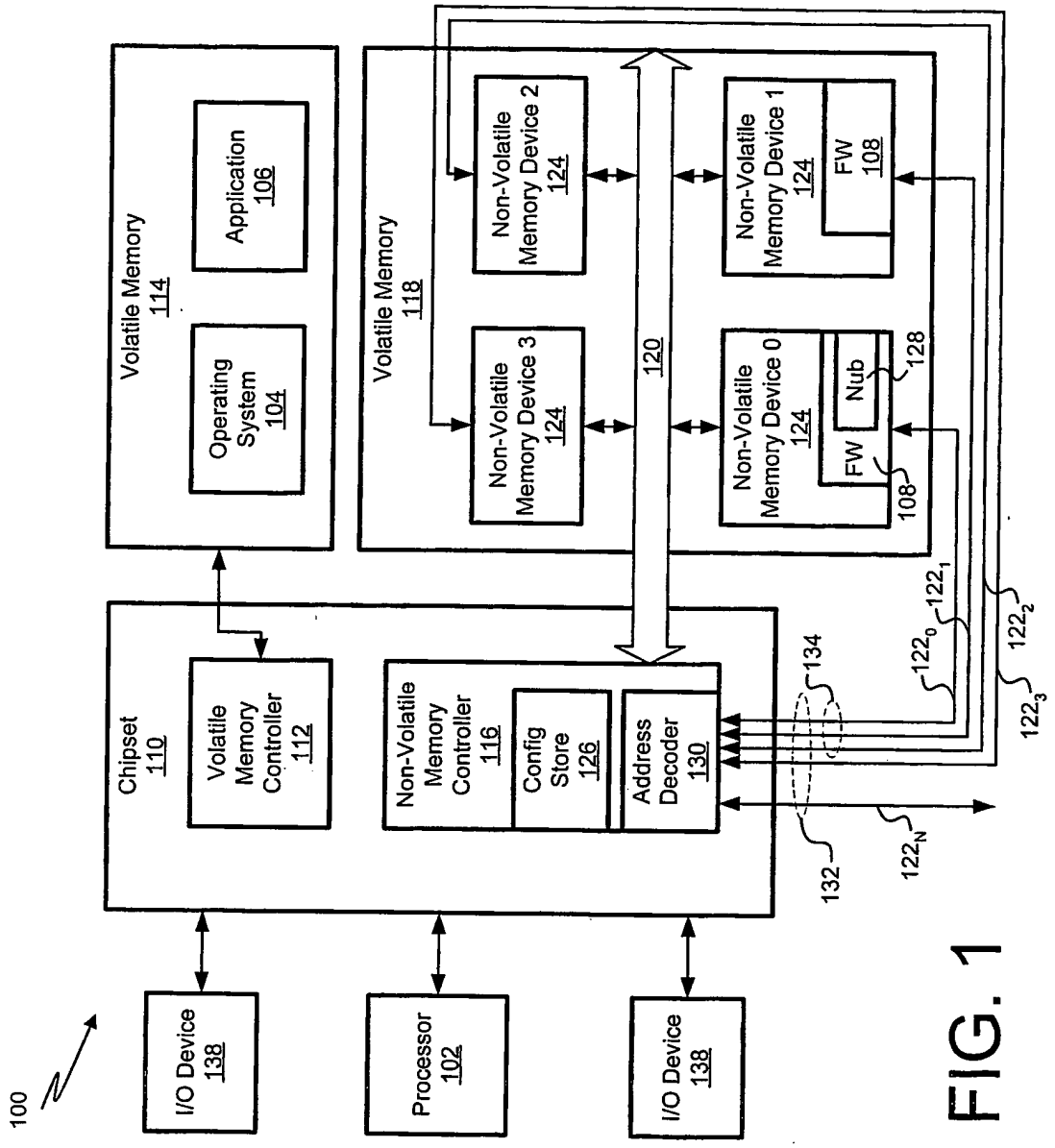
100
I/O Device 138
Processor 102
I/O Device 138
Chipset 110
Volatile Memory Controller 112
Non-Volatile Memory Controller 116
Config Store 126
Address Decoder 130
Volatile Memory 114
Application 106
Operating System 104
Volatile Memory 118
Non-Volatile Memory Device 2 124
Non-Volatile Memory Device 1 124
FW 108
Non-Volatile Memory Device 3 124
Non-Volatile Memory Device 0 124
Nub
128
FW
108
120
134
132
122N
1220
1221
1222
1223

FIG. 1

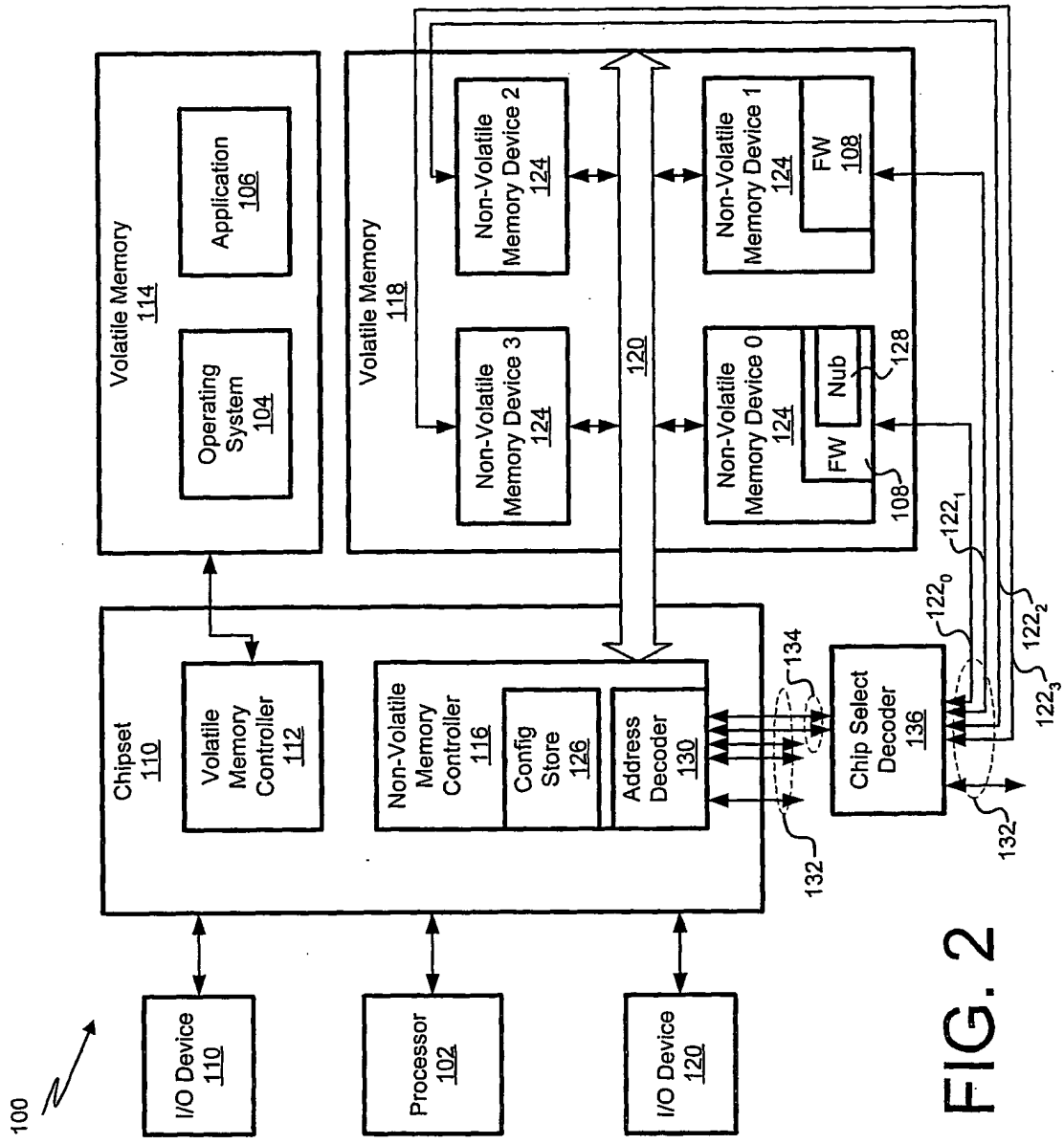
100
I/O Device 110
Processor 102
I/O Device 120
Chipset 110
Volatile Memory Controller 112
Non-Volatile Memory Controller 116
Config Store 126
Address Decoder 130
134
132
Chip Select Decoder 136
122_0
122_1
122_2
122_3
132
Volatile Memory 114
Operating System 104
Application 106
Volatile Memory 118
Non-Volatile Memory Device 2 124
Non-Volatile Memory Device 1 124
FW 108
Non-Volatile Memory Device 3 124
120
Non-Volatile Memory Device 0 124
Nub
128
FW
108

FIG. 2

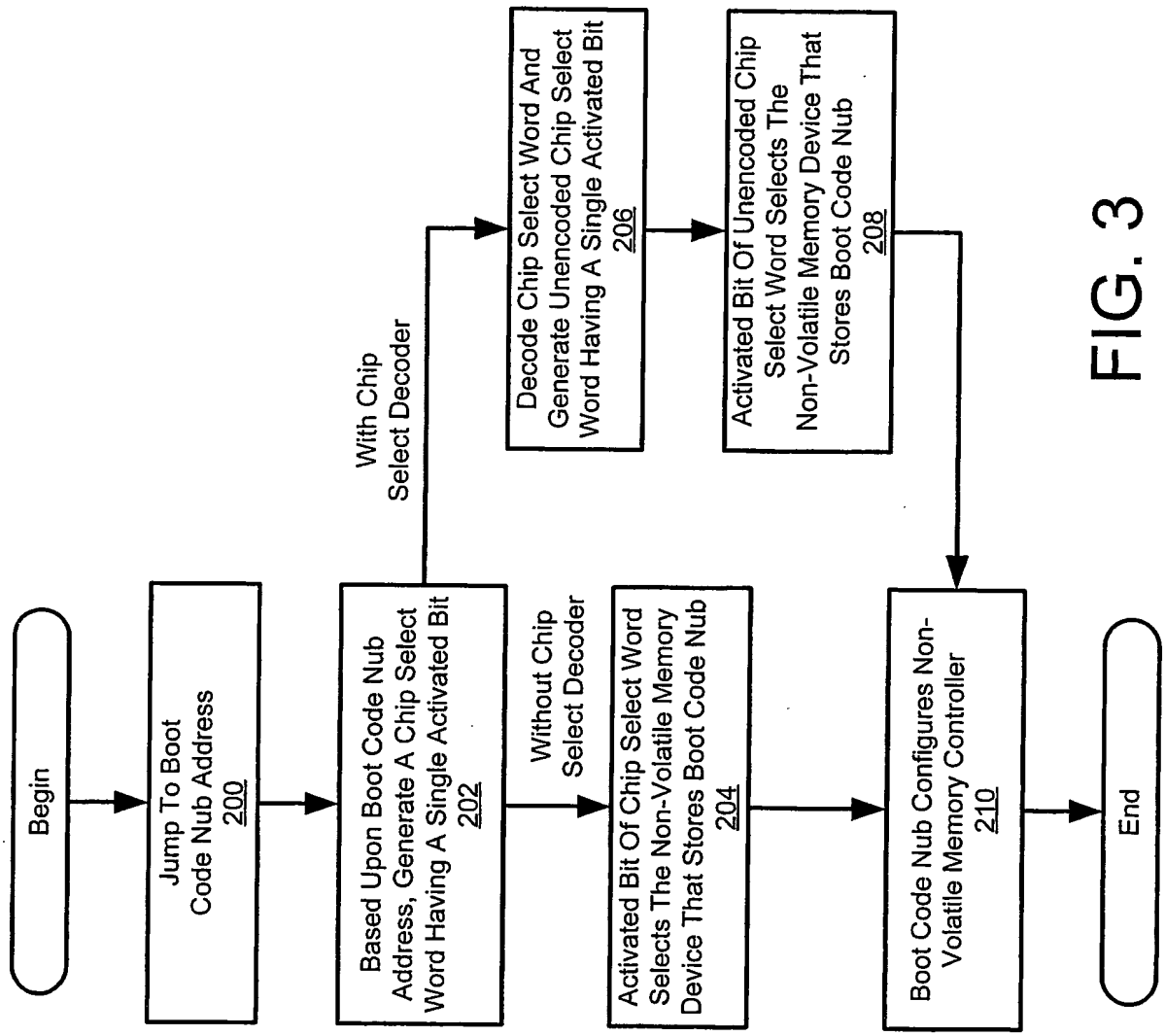
Begin
Jump To Boot Code Nub Address 200
Based Upon Boot Code Nub Address, Generate A Chip Select Word Having A Single Activated Bit 202
With Chip Select Decoder
Decode Chip Select Word And Generate Unencoded Chip Select Word Having A Single Activated Bit 206
Activated Bit Of Unencoded Chip Select Word Selects The Non-Volatile Memory Device That Stores Boot Code Nub 208
Without Chip Select Decoder
Activated Bit Of Chip Select Word Selects The Non-Volatile Memory Device That Stores Boot Code Nub 204
Boot Code Nub Configures Non-Volatile Memory Controller 210
End

FIG. 3